Implementation of an All-Optical Time-Slot-Interchanger Architecture

O. Zouraraki, K. Yiannopoulos, P. Zakynthinos, D. Petrantonakis, E. Varvarigos, A. Poustie, G. Maxwell, and H. Avramopoulos

***Abstract*—We demonstrate a wavelength-converter-based optical time-slot-interchanger. It consists of three cascaded programmable delay stages and employs the first hybrid integrated, on a chip, quadruple array of semiconductor optical amplifier Mach–Zehnder interferometer switches. It exhibits error-free operation with 10-Gb/s nonreturn-to-zero packets and a power penalty of 1.8 dB.**

***Index Terms*—Mach–Zehnder interferometer (MZI), optical buffering, time-slot interchanger.**

I. Introduction

THE capability to rearrange the order of optical packets in programmable fashion is a key issue that still has to be addressed towards the realization of high-speed optical-packet-switched (OPS) nodes, since it enables crucial functionalities such as contention resolution and traffic shaping. This capability has been extensively investigated in architectures that incorporate optical switches and feedback/feed-forward fiber delay lines [1], and recent advances in optical integration have enabled the demonstration of a fully integrated system [2]. A practical and simple means for rearranging the packet order are time-slot-interchangers (TSIs)[3], [4], in which packets experience programmable delays that have been determined by the node control plane so that packets do not content at the node output. One option for the implementation of optical TSIs is to use semiconductor optical amplifier Mach–Zehnder interferometer (SOA-MZI) gates. The SOA-MZI high-speed processing capability and integrability into compact arrays [5] allows the design of optical TSIs that employ cascades of switching elements. The packet rearranging capabilities of SOA-MZI-based TSIs are limited by the total number of gates that can be integrated on a chip. However, recent studies show that transfer control protocol over OPS networks provides almost full link utilization, if packet rearranging capability for as small as a few tens of packets is provided [6]. As such, it is expected there will be no real need for large-scale packet rearranging capability in future OPS networks.

Manuscript received December 28, 2006; revised June 1, 2007. This work was supported by the European Commission through Project IST-MUFINS (FP6-004222) and Project IST-ePhoton/One+, and by the EPEAEK, PYTHAGORAS II Program.

O. Zouraraki, P. Zakynthinos, D. Petrantonakis, and H. Avramopoulos are with the School of Electrical and Computer Engineering, National Technical University of Athens, Zografou 15773, Greece (e-mail: ozour@mail.ntua.gr).

K. Yiannopoulos and E. Varvarigos are with the Department of Computer Engineering and Informatics, University of Patras, Rio 26500, Greece.

A. Poustie and G. Maxwell are with the Centre for Integrated Photonics, Adastral Park, Ipswich IP5 3RE, U.K.

Digital Object Identifier 10.1109/LPT.2007.902331

Within this context, we demonstrate a multiple-stage TSI scheme that requires a small number of optical switches. Each TSI stage employs a wavelength-selectable converter (WSC) and feed-forward delay lines. The TSI architecture has been based on a precise algorithm described in detail in [7]. For a given number of interchanging packets, this algorithm takes advantage of the available wavelengths so as to minimize the number of required stages and WSCs. In the present implementation, we show full interchange capability of four packets using a three-stage architecture. The WSCs were implemented on the first ever fabricated quadruple switch array of SOA-MZIs on a single chip. The scheme shows error-free rearranging of four 10-Gb/s nonreturn-to-zero (NRZ) packets, with a power penalty of 1.8 dB.

II. Concept and System Architecture

In order to ease our design description, we start by assuming that the data stream is divided and arranged into time frames, that contain a number of time slots and that each packet occupies a time slot. In our present implementation, each time frame contains four time slots, so that our TSI structure can rearrange at most four packets that have arrived within a time frame. At the TSI output, each incoming packet may be placed on any of the four available time slots. The worst-case scenario is depicted in Fig. 1(a) where the first packet (packet A) and the last packet (packet D) need to interchange their positions in the time frame. In this case, packet D should get zero time-slot delay while packet A should get six time-slots delay. For other packet rearrangement cases, intermediate values of delay are necessary. This means that the TSI should be capable to provide all possible delays between zero and six time slots, namely a total of seven different delays. Supposing that the TSI is implemented in a single-stage configuration, like the one depicted in Fig. 1(b), seven wavelengths will be necessary. This is a result of the assignment of a specific delay to a particular port of the wavelength demultiplexer, so that a packet can access this delay by appropriate wavelength conversion at the WSC. Unfortunately, the single-stage TSI implementation approach does not scale well in terms of required wavelengths. For instance, the rearrangement of the packets in a ten-packet time frame requires 19 wavelengths and for the general case of N packet time frames, $2N-1$ wavelengths have to be used.

To overcome this poor scaling property of the single-stage TSI in terms of number of wavelengths, a multistage implementation may be adopted. With such implementation, each stage will use less than seven wavelengths and successive stages will have a different set of delays. As such, each stage will be able to interchange less than the four packets of the frame at once. However, the action of successive interchange stages can perform full packet rearrangement as proven in [7], where a full

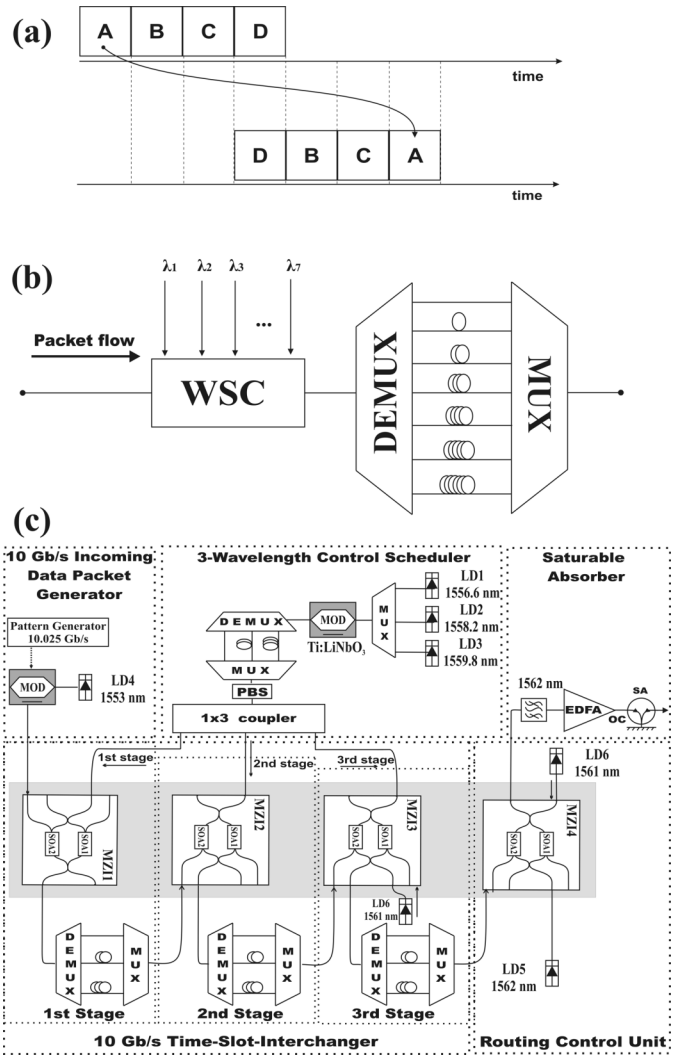

Fig. 1. (a) Worst-case scenario for the interchanging of four packets; (b) single-stage time-slot interchanger; and (c) experimental setup.

description of the design algorithm and its advantages is presented. The number of the required TSI stages and wavelengths per stage, as well as the delay times they introduce, are interrelated design parameters derived from the algorithm as a function of time slots assigned to each frame. In this respect, for a given number of time slots per frame, it is possible to optimize the number of TSI stages to minimize the number of WSC so as to contain signal degradation due to consecutive wavelength conversions and cost.

Table I summarizes the number of required wavelengths versus the time slots per frame for TSIs that comprise one, three, and five stages. Clearly, the three-stage design we demonstrate scales well with the number of available wavelengths. For instance, only 13 wavelengths are required for approximately 49 packets, contrary to the single-stage TSI that would require almost 100. Still, additional stages are required to further extend the rearranging capabilities of the TSI architecture, with a possible decrease in the required wavelengths. For a five-stage design, a mere seven wavelengths are required for interchanging up over 49 packets.

TABLE I
NUMBER OF REQUIRED WAVELENGTHS VERSUS TIME SLOTS PER FRAME FOR TSIS THAT COMPRISE ONE, THREE, AND FIVE STAGES

Interchangeable timeslots	Required Wavelengths		
	s=1	s=3	s=5
4	7	3	3
9	17	5	5
16	31	7	5
25	49	9	5
36	71	11	7
49	97	13	7

III. EXPERIMENTAL SETUP

The experimental demonstration of the proposed architecture is shown in Fig. 1(c). It consists of the 10-Gb/s NRZ data packet generator, the three-wavelength control scheduler, the 10-Gb/s TSI circuit, the routing control unit, and a fiber coupled saturable absorber (SA) mounted on a circulator. The wavelength control scheduler involves three continuous-wave signals (1556.6, 1558.2, 1559.8 nm) which are multiplexed and modulated into packet envelopes that coincide in the time domain. These envelopes are introduced into a delay configuration comprising Demux/Muxes and fiber segments of fixed length. A sequence of three consecutive packet envelopes of same-length and different-wavelength is thus obtained at the Mux output. This signal enters then a polarization beam splitter (PBS) so that a specific polarization component from the three wavelengths to be picked out and then split into three parts which form the input signals of the three stages of our circuit. The 10-Gb/s incoming data packet generator employs a 1553-nm laser and a modulator to generate a sequence of 10.025-Gb/s NRZ $2^7 - 1$ pseudorandom bit sequence data packets which are injected into the first stage of the TSI. Each TSI stage deploys an SOA-MZI switch and a Demux/Mux-based programmable delay bank. The MZI operates as a wavelength converter, based on cross-phase-modulation effect caused by the control signal, assigning each packet that appears at its control port with one of the three input wavelengths. The delay bank delays each incoming packet according to the wavelength it has been assigned. As a result, incoming packets are interchanged at the stage output based upon the wavelength assignment procedure. The fiber segments of each delay bank correspond to zero, one, and two time slots for the first stage, zero, two, and four time slots for the second stage, and zero, one, and two time slots for the third stage. In our implementation, each time slot corresponds to 80-cm fiber. With those delays, the TSI system is demonstrated to be no blocking in terms of at the output of each stage no two packets assert the same time slot. The wavelength-converted packets at each stage output are fed to the control port of the next stage MZI in a counterpropagating control/input signal fashion except for the first stage. The fourth MZI acts as a routing control unit that translates the three-wavelength output of the TSI to a single wavelength (1562 nm) for appropriate routing in a wavelength-routed node. A holding beam at 1561 nm enters MZI 3 and MZI 4 to reduce amplified spontaneous emission (ASE) and increase the extinction ratio of the output signals. The four MZIs belong to a quadruple SOA-MZI array hybrid integrated on a single chip. Finally, the SA with resonant wavelength at 1561 nm is used at

TABLE II
POWER/ENERGY REQUIREMENTS OF MZI SWITCHES

MZI	Input Power	Control Energy	Holding Beam Power
1st Stage (MZI1)	2.3 dBm	1.61 pJ	-
2nd Stage (MZI2)	0.5 dBm	1.39 pJ	-
3rd Stage (MZI3)	-0.04 dBm	1.57 pJ	-1.6 dBm
Routing Control Unit (MZI4)	8.1 dBm (CW)	1.48 pJ	-1 dBm

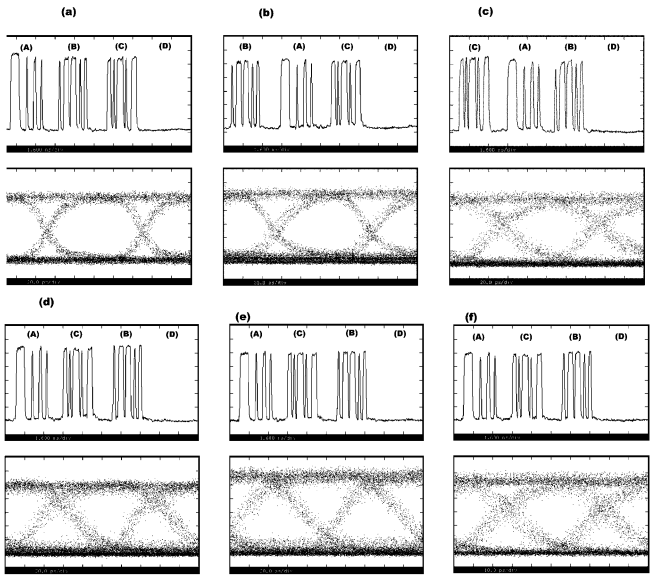

Fig. 2. Oscilloscope traces and respective eye diagrams of (a) input data packets, (b) first-stage output, (c) second-stage output, (d) third-stage output, (e) routing control unit, and (f) SA output. The time base is 1.6 ns/div for the oscilloscope traces and 20 ps/div for the eye diagrams.

the setup output to enhance the signal quality through noise reduction and pulse narrowing. Table II summarizes the power/energy requirements for the four MZIs.

IV. RESULTS AND DISCUSSION

Fig. 2 illustrates the time-domain evolution and the corresponding eye diagrams of optical packets at each stage of the TSI circuit. In particular, Fig. 2(a) shows the input signal consisting of four 40-bit-long time slots. The first three time slots (A, B, C) accommodate 25-bit 10-Gb/s synchronous data packets followed by 15 zero bits, while the fourth time slot (D) is empty. Fig. 2(b) depicts the first stage output. The original time-slot sequence $\{A, B, C, D\}$ is transformed to $\{B, A, C, D\}$, after interchanging A and B. This corresponds to A being delayed by two time slots, B not being delayed, and C and D being delayed by one time slot. The sequence $\{B, A, C, D\}$ is similarly transformed to $\{C, A, B, D\}$ with time slots A, B, C, and D acquiring delay of two, four, zero, and two time slots, respectively, as in Fig. 2(c). Equally, A and C are exchanged at the third stage forming the sequence $\{A, C, B, D\}$. Finally, Fig. 2(e) and (f) show the output of the routing control unit and the SA, respectively. Fig. 3 demonstrates the bit-error-rate (BER) measurements obtained at the output of each stage. Error-free operation was achieved with

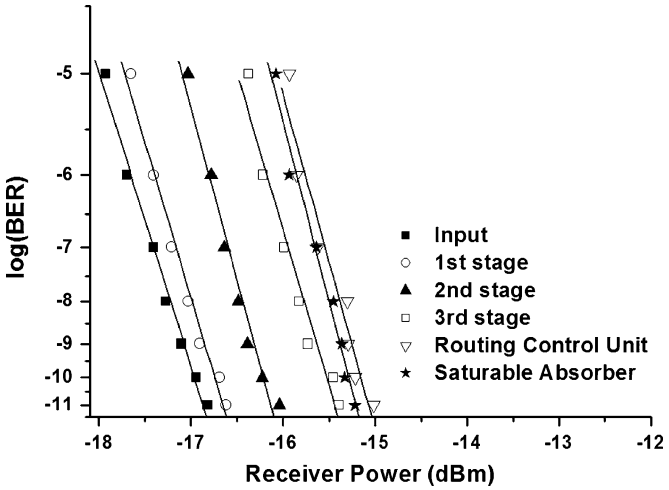

Fig. 3. BER measurements.

power penalties of 0.2, 0.78, 1.43, and 1.8 dB after the first, second, third TSI stages and the routing control unit, with respect to the input signal. The gradually increasing power penalty is primarily a result of eye closure due to pulse broadening from the gain saturation and recovery dynamics of the SOAs. This effect is partially offset by the SA, which narrows the pulse and enhances the extinction ratio. The corresponding BER curve exhibits a negative power penalty of -0.2 dB with respect to the output of the routing control unit. Better performance of the demonstrated setup is expected with the use of return-to-zero pulses and the push–pull technique to limit the SOA-MZI switching window.

V. CONCLUSION

We have demonstrated a wavelength-converter-based optical TSI. It consists of three cascaded programmable delay stages and employs the first hybrid integrated, quadruple array of MZI switches. Error-free operation was achieved at 10 Gb/s with a power penalty of 1.8 dB. The proposed architecture could be used for contention resolution and traffic shaping in OPS networks.

REFERENCES

[1] D. K. Hunter, M. C. Chia, and I. Andonovic, "Buffering in optical packet switches," *J. Lightw. Technol.*, vol. 16, no. 12, pp. 2081–2094, Dec. 1998.

[2] E. F. Burmeister and J. E. Bowers, "Integrated gate matrix switch for optical packet buffering," *IEEE Photon. Technol. Lett.*, vol. 18, no. 1, pp. 103–105, Jan. 1, 2006.

[3] Z. Pan *et al.*, "All-optical programmable time-slot Interchanger using optical-label switching with tunable wavelength conversion and N by N arrayed waveguide grating routers," in *Proc. OFC*, 2002, pp. 267–268.

[4] Z. Wang, N. Chi, and S. Yu, "Time-slot assignment using optical buffer with a large variable delay range based on AVC crosspoint switch," *J. Lightw. Technol.*, vol. 24, no. 8, pp. 2994–3001, Aug. 2006.

[5] P. Zakynthinos *et al.*, "Single chip quad MZI array in a 40 Gb/s AOLS front-end," in *Proc. OFC*, 2007, Paper OWH7.

[6] N. Beheshti, Y. Ganjali, R. Rajaduray, D. Blumenthal, and N. McKeown, "Buffer sizing in all-optical packet switches," in *Proc. OFC*, 2006, Paper OThF8.

[7] K. Yiannopoulos, E. Varvarigos, and K. Vlachos, "Multiple-input buffer and shared buffer architectures for optical packet and burst switching networks," *J. Lightw. Technol.*, vol. 25, no. 6, pp. 1379–1389, Jun. 2007.