ARTEMIS: 40-Gb/s All-Optical Self-Routing Node and Network Architecture Employing Asynchronous Bit and Packet-Level Optical Signal Processing

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***Abstract*—A 40-Gb/s asynchronous self-routing network and node architecture that exploits bit and packet level optical signal processing to perform synchronization, forwarding, and switching in the optical domain is presented. Optical packets are self-routed on a hop-by-hop basis through the network by using stacked optical tags, each representing a specific optical node. Each tag contains necessary control signals for configuring the node-switching matrix and forwarding each packet to the appropriate outgoing link and onto the next hop. In order to investigate the feasibility of their approach physical-layer simulations are performed, modeling each optical subsystem of the node showing acceptable signal quality and end-to-end bit error rates. In the All-optical self-RouTer EMploying bIt and packet-level procesSing (ARTEMIS) control plane, a timed/delayed resource reservation-based signaling scheme is employed combined with a load-balancing feedback-based contention-avoidance mechanism that can guarantee a high performance in terms of blocking probability and end-to-end delay.**

***Index Terms*—All-optical logic gate, all-optical signal processing, asynchronous traffic, feedback-based protocols, optical-burst switching (OBS), optical packet switching, self-routing, semiconductor optical amplifier (SOA), timed/delayed reservation.**

I. Introduction

THE MIGRATION from current wavelength division multiplexing (WDM) networks employing a circuit-switching technology to optical packet switched networks has been identified as a key issue, since the former cannot provide a bandwidth-on-demand and are not suitable for "greedy" applications involving bursty traffic [1]. To draw this migration path, the attention has been focused on the identification of the functionalities required in a packet switched node and how these could be best carried out in the optical domain [2]. Signal conditioning, synchronization, and routing have been identified as the main classes of operations that should be performed in order to be able to switch optical packets in a photonic network. As far as signal conditioning and synchronization is concerned, electronic circuits have been presented performing various functionalities including data regeneration [3], clock recovery [4], and data recovery [5], [6]. The routing functionalities such as address recognition [7] or buffering [8] are considered to be straightforward processes when handled in the electrical domain [9]. For example, address recognition is usually performed by loading the address into a register and comparing it with a stored bit pattern. However, for very high bit rates, the storage and random access of an address in a register cannot be considered as a trivial process.

The application of optical signal processing techniques for packet switching applications has become feasible due to the development and commercialization of optical logic elements, such as optical gates and interferometric switches [10]. These optical logic elements are suitable for a high-speed signal processing and they have already been established as the fundamental building blocks of all-optical switching nodes [11]. In this context, all-optical gates have been used as core elements performing a diversity of network functionalities, such as wavelength conversion [12], data regeneration [13], [14], clock recovery [15], [16], header from payload separation [17], [18], header matching [7], and data recovery [19].

Despite the above achievements, integration of functionalities in a system environment to perform lossless packet processing and routing in the optical domain still remains an elusive target. The routing plane is the most demanding in terms of intelligence required in the optical layer and the limitations imposed primarily stem from the lack of an optical random access memory capable of storing information. As a consequence, the node local-address-generation procedure is difficult and does not scale well with increased number of header bits when implemented with fiber delay lines. In addition, the lookup table cannot be implemented with a current photonic technology, although revolutionary research has been reported [20]–[22], which could initiate an evolution path towards photonic random access memory.

As optical buffers are far from practical and given the lack of the optical random access memory, there has been considerable attention towards the design and implementation

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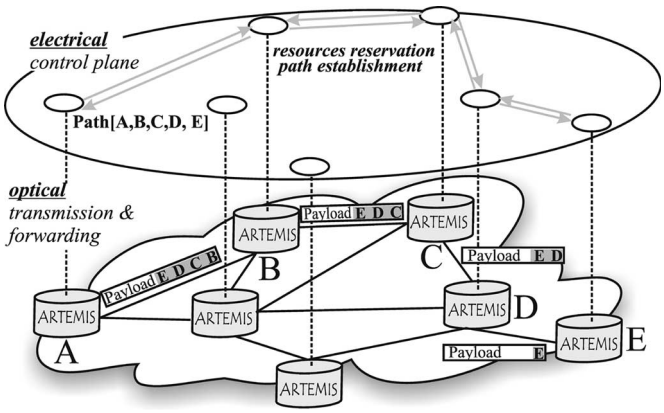

Fig. 1. ARTEMIS network architecture and all-optical burst forwarding.

of bufferless self-routing switches as a solution to eliminate optical/electrical/optical (O/E/O) conversions associated with packet address reading and routing. In a self-routing-network scenario, the intermediate nodes forward the incoming packets to the appropriate output ports according to a routing information embedded at the source node. The case where the routing decisions are made on the basis of a single-bit information in the header is also referred to as bit-level packet switching (BLPS) [23] and employs an optical processing of the header. Although self-routing offers simple routing control in an optical packet switched network node, its implementation imposes specific requirements concerning the operation of the optical logic circuits involved. More specifically for an all-optical self-routing node to operate, it is of vital importance to be able to generate the optical signals controlling the node gates in order to achieve routing on a packet by packet basis through the switching matrix. This implies that each packet should be handled as an independent entity and the control signals generated should persist only for the duration of each data packet. To address these issues self-routing techniques employing self-clocking [24], all-optical address recognition [23], and serial-to-parallel conversion-based label recognition [25] have been demonstrated. Self-clocking requires that each packet carries its own clock, posing specific requirements for the transmitters, whereas its operation is extremely sensitive to linear or nonlinear distortion due to fiber propagation. The approach reported in [25] requires an electronic processing plane for label recognition, whereas the switching matrix is also electronically controlled. More recently, an all-optical self-routing switch suitable only for a slotted operation in ring network topologies has been presented [26] employing simple, all-optical header processing using injection locking in Fabry–Pérot laser diodes. This scheme performs simple on/off switching and its operation relies on using different power levels in the control signals, which makes it susceptible to the physical impairments induced during propagation through the network links.

In this communication, we propose and evaluate a self-routing-network architecture, ARTEMIS, which is able to perform successfully without the intervention of electronics and avoiding the need for optical header recognition and decoding in each node by using simple all-optical circuits. The primary goal of ARTEMIS is to achieve packet switching with bit-level processing, hence exploiting the performance of optical gates at very high data rates. The self-configuration of an ARTEMIS node is achieved as all the routing decisions are performed on-the-fly using information embedded in the packet header, thus avoiding O/E/O conversions or local address generation and all-optical header recognition. The designed switch inherently operates on a packet-by-packet basis and is capable of routing 40-Gb/s asynchronous packets, adding flexibility and true transparency to the network. In addition, the node is self-synchronizing and, thus, does not require a phase synchronization with local electrical or optical oscillators. In addition, ARTEMIS node does not require multilevel coding schemes or specially modulated payload or headers for correct operation. When the proposed switch architecture is used in conjunction with a suitable resource reservation scheme for contention protection and appropriate load-balancing algorithms, it can provide high throughput and low blocking ratio and can potentially eliminate the data flow bottlenecks at the routing controller avoiding the time consuming search and updating of look-up tables.

II. ARTEMIS Network Architecture

The self-routing-network architecture proposed is shown in Fig. 1 and consists of two clearly defined layers. All network functionalities associated with transmission, regeneration, and routing are performed in the optical layer. The control plane is solely responsible for resources reservation for contention protection. The transmission of optical packets through the ARTEMIS network is realized using optical headers that contain stacked optical "tags" [27], each corresponding to a specific node. In addition, each optical tag contains bit-level information for optically controlling the switching matrix of the node and thus routing the data packet to the appropriate outgoing link and on to the next hop.

In this network scenario, when a transmission request is made, appropriate control communication is initiated to allocate the required resources and establish a connection between two ARTEMIS nodes (e.g., A and E, as shown in Fig. 1). In order to tackle issues such as contention, bandwidth efficiency, and capacity utilization while fulfilling the requirement for no buffering in the self-routing network, timing information is used to schedule the data flows and reserve complete lightwave switched paths (LSPs). For the configuration of each ARTEMIS node, an optical header is embedded in the packet containing all node hops (tags) according to the computed path and the transmission commences. Upon arrival to the next node, the first tag is all-optically removed and the packet is forwarded to the appropriate outgoing link of the node by the control signals embedded within the specific tag "B," as described in [28] and [29]. In contrast to these approaches routing within the ARTEMIS node is performed in the time-domain using optically controlled 1×2 all-optical elements and not wavelength conversion as in [29]. Equivalently, by using the stacked tags as control signals within each node, the packet is self-routed through the network, until the destination node is reached and the packet is directed onto the "drop" port of "E."

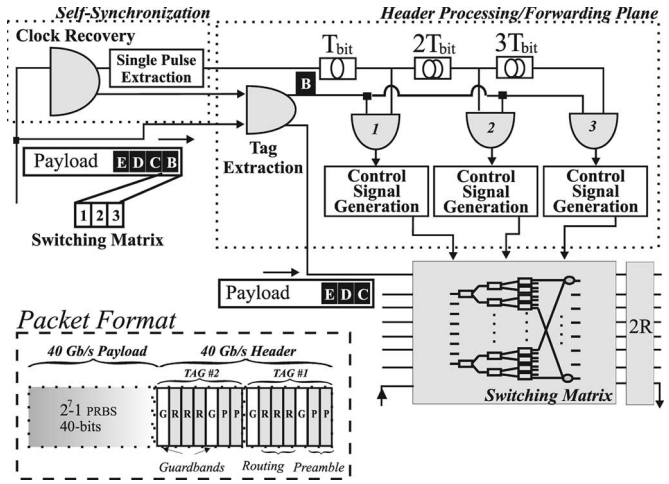

Fig. 2. ARTEMIS node physical-layer implementation. Inset shows the packet format used for the simulation of ARTEMIS node operation consisting of two optical tags each containing three routing bits for controlling 8×8 switching matrices.

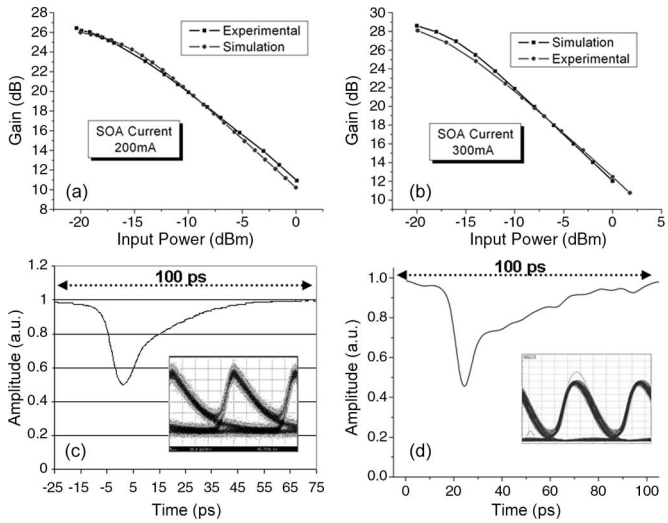

Fig. 3. Comparison between simulation and experimental results. SOA gain response when operated at (a) 200 mA and (b) 300 mA. Recovery time measurements (c) provided by supplier and (d) using the simulation model. Insets show 10-Gb/s wavelength conversion results from experiment and simulation.

III. ARTEMIS Physical-Layer Node Design and All-Optical Subsystem Modeling

The physical-layer implementation of an ARTEMIS node is shown in Fig. 2 and consists of the self-synchronization stage, the all-optical header-processing plane, and the switching matrix. The synchronization stage provides the necessary clock signals that are self-extracted from the incoming data packets. The header-processing/forwarding plane is responsible for all-optically processing the extracted packet tags and generating suitable control signals that are used to drive the all-optical switching elements within the switching matrix of the node.

The complete ARTEMIS node was designed and simulated using the commercially available simulation tool VPI TransmissionMaker. In order to achieve high accuracy and good agreement with experimental results, the model chosen used a time-domain analysis of bidirectional optical fields within all active devices of ARTEMIS node. The semiconductor optical amplifier-based Mach–Zehnder interferometer (SOA-MZI) model was specifically designed to closely match the experimental behavior of the 40-Gb/s reshaping and regeneration (2R) regenerator prototypes developed by Center for Integrated Photonics (CIP, U.K.). Fig. 3 shows the comparative results between experimental data and simulated results for the device. Specifically, Fig. 3(a) and (b) shows static gain measurements of the SOAs used within the interferometric structure of the optical gates, showing a good agreement. Additionally, Fig. 3(c) and (d) show pump-probe measurements for characterizing the gain recovery time of the SOAs. The recovery time provided by the supplier and from the simulation was 25 and 30 ps, respectively. The inset of the figure also shows eye diagrams for 10-Gb/s wavelength conversion obtained experimentally and from simulation. The data pulses were pseudorandom bit sequence (PRBS) $2^7 - 1$ with 11-ps temporal width and 11-dBm peak power, whereas the probe signal power level was -7 dBm. The response time was measured 25 and 23 ps at 1/e point, experimentally, and using the simulation model, respectively.

A. ARTEMIS Packet Format and Guardbands Required

As briefly described in Section II, ARTEMIS all-optical forwarding concept is based on stacked optical tags that each contain all necessary bits for controlling the switching matrix of each node. Fig. 2 shows the packet format required for correct operation and consists of an optical header and payload both serially encoded at 40 Gb/s. The modulation format must be return to zero (RZ) in order for correct operation within the optical gates of ARTEMIS node. The optical header consists of a number of stacked optical tags each representing an ARTEMIS node. The number of stacked tags depends on the number of hops within the network and they are embedded by the control plane after the burst assembly process in the ingress node (IN). Each tag contains a control signal that is a serially encoded binary word, used to set the switches within the node switching matrix. The guardband requirements for correct packet self-routing are also showed in the inset of Fig. 2. Specifically, two preamble bits (50 ps) are inserted in front of each tag within the header field to assist clock extraction at each ARTEMIS node. Additionally, in accordance with the principle of operation of the tag extraction subsystem, one guardband bit (25 ps) is inserted between the payload and the routing bits to account for the clock acquisition time of the self-synchronization stage. This ensures correct tag extraction by avoiding incomplete switching of the tag during the rise time of the clock. Specifically, for the demonstration of ARTEMIS principle of operation, the packet format used in all simulation studies is shown in the inset of Fig. 2. The 40-Gb/s optical packet consists of a 40-bit long payload encoded with part of a $2^7 - 1$ PRBS sequence. The optical header includes two stacked tags each containing binary routing bits and guardbands required by the synchronization and header-processing stages of the node. Each tag has three embedded routing bits responsible for controlling the switching matrix of the node that consists of 1×2 optically controlled optical gates. Two

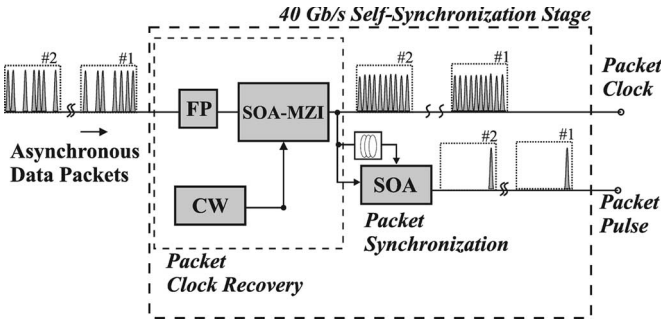

Fig. 4. Self-synchronization stage consisting of a 40-Gb/s packet clock recovery and a packet synchronization subsystem.

preamble bits are also included at the start of each tag to assist the clock recovery process in each hop. Further, single-bit guardbands are inserted between each tag and payload as required by the all-optical tag extraction subsystem [18]. In order to investigate the cascadeability of the approach, the switching matrix was assumed to be a strictly nonblocking 8×8 switch, where the optical packet propagates through three cascaded 1×2 optical switching elements. The ARTEMIS node can handle short asynchronous and fixed-length packets with low guard band requirements. Successful all-optical processing of variable-length packets is still possible provided that the spacing of each packet is fixed and equal to the largest packet within the ARTEMIS network.

B. All-Optical Synchronization Stage

Fig. 4 shows the schematic diagram of the proposed self-synchronization stage illustrating the two functionalities required namely clock extraction at the line rate and single pulse extraction at the packet rate. The 40-Gb/s all-optical clock recovery proposed [16] and simulated for the ARTEMIS node consists of a passive comb-generating filter for retiming and a saturated nonlinear gate for reshaping. Combination of the two elements results in the self-extraction of clock packets suitable for controlling additional optical gates within the node. The reason of choosing the specific clock recovery scheme is its ability to perform clock extraction on a per-packet basis without requiring any synchronization to local oscillators, fact that can lead to packet-format transparency [30]. The comb-generating filter used was a Fabry–Pérot filter with Finesse 20 and free spectral range equal to the line rate. Exploiting the short memory effect of the filter, incoming data packets are transformed to clock-resembling packets. This generated signal, however, suffers from intense pulse-to-pulse amplitude modulation that is removed by utilizing a saturated optical gate as a pulse-to-pulse equalizer [31]. The optical gate was simulated as a SOA-MZI capable of operating at 40 Gb/s. An experimental performance evaluation of the 40-Gb/s clock recovery utilized can be found in [16].

The second synchronization subsystem is responsible for producing a single optical pulse per incoming data packet, without the intervention of any electronic circuitry. As shown in Fig. 5, the packet synchronization subsystem consists of a single SOA and exploits cross gain modulation (XGM) effect to

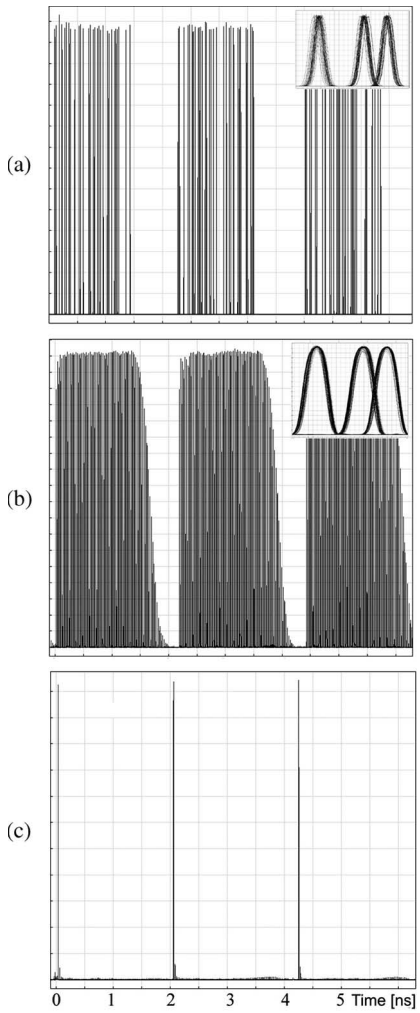

Fig. 5. (a) Incoming 40-Gb/s asynchronous data packets, (b) corresponding recovered clock packets, and (c) extracted pulse per incoming packet at 500 ps/div timebase. Insets show asynchronous eye diagrams obtained.

achieve the required optical functionality. The recovered packet clock is inserted both as the probe and pump signal with a single bit offset in a counter-propagating fashion. Due to the specific temporal synchronization of the interacting signals, only the first clock-pulse experiences amplification, whereas subsequent probe pulses are suppressed through the strong counter-propagating pump signal incident on the SOA.

Fig. 5 shows simulation results of the 40-Gb/s self-synchronization stage obtained. Specifically, Fig. 5(a) illustrates three asynchronous packets with packet format according to Section III-A suffering from 0.8 dB and 500 fs amplitude and timing jitter, respectively. When the incoming data enter the self-synchronization stage of the node, clock extraction on a per-packet basis is achieved. Hence, a packet clock with instant locking and short decay time is self-extracted from each incoming data packet, as shown in Fig. 5(b). Finally, the extracted clock packets are inserted into the packet synchronizer and a single pulse per incoming packet is generated at the output [Fig. 5(c)]. The extracted clock packets exhibited 0.25 dB and 277 fs amplitude and timing jitter, and the extracted pulse had an extinction ratio of more than 14 dB.

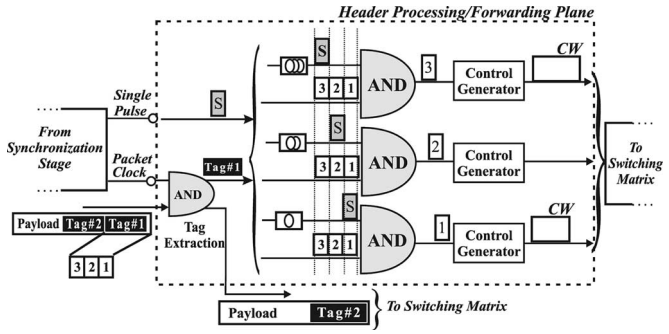

Fig. 6. Detailed schematic diagram of the header-processing/forwarding plane.

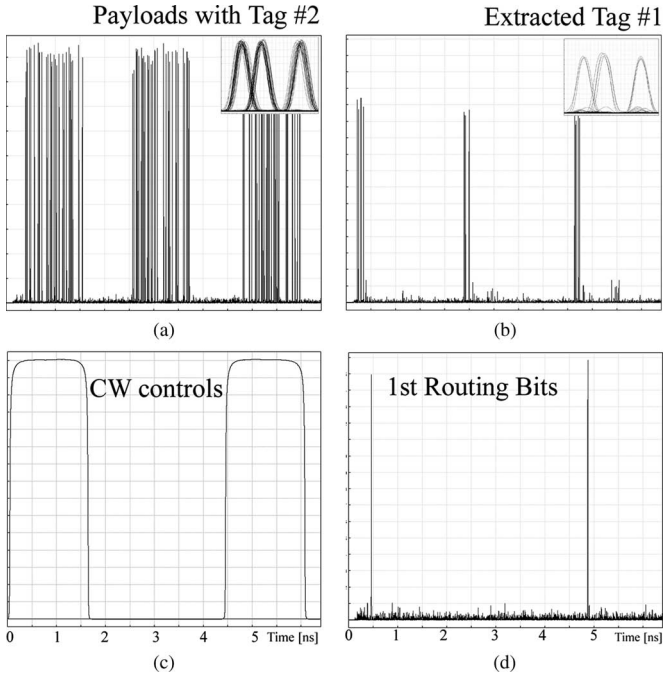

Fig. 7. Simulation results of 40 Gb/s (a) extracted payload and remaining tag, (b) extracted tag #1, (c) generated CW control according to (d) extracted routing bit of each packet.

C. All-Optical Header-Processing/Forwarding Plane

This part of the node includes three distinct all-optical functionalities: the tag extraction, the routing bit extraction and the control-signal generation. The principle of operation of the complete header-processing plane is presented in the schematic diagram of Fig. 6. The incoming optical packet and the recovered packet clock stream enter the tag extraction gate that consists of an SOA-MZI gate configured as a Boolean AND gate [18]. The temporal synchronization of the two signals is such that the first optical tag (tag #1) lies outside the switching window defined by the recovered packet clock. Hence, the whole payload, including tag #2, are switched, whereas only tag #1 remains unswitched and enter the header-processing/forwarding plane. Having separated the optical tag from the remaining payload, tag #1 is then fed into an array of SOA-MZI gates, each responsible for extracting a single-routing bit, with the help of the single pulse extracted at the self-synchronization stage. By imposing a single bit of optical delay to the single pulse that is fed as control signal, a single-routing bit is switched at the output of each optical gate. Finally, each routing bit enters the control-signal-generation block and depending on its binary value, a control signal is generated and forwarded to the switching matrix. The optical functionality required for the control-signal generator is the transformation of bit-level signal into a packet-level signal by exploiting an optical-element-exhibiting memory. Hence, a single optical bit at the input of the control-signal generator must be capable of producing a continuous wave (CW) or pulsed packet with duration equal to the total packet length, as shown in Fig. 7. There are three distinct ways of implementing such a control-signal generator using an optical flip-flop [20], an optical circuit with finite memory [32], or an electronic pulse generator followed by an optoelectronic conversion [25]. In order to reduce the complexity of the simulation model, the control-signal generator was implemented by using an electrical pulse generator after the optoelectronic conversion.

The complete header-processing plane was simulated and Fig. 7 shows typical results obtained at 40 Gb/s. Fig. 7(a) and (b) shows the two outputs of the tag extraction optical gate. The resulting pulsewidth at the output of the gate was measured 2.6 ps, due to the propagation within the SOA and the 200-GHz bandpass filter used for rejecting amplified spontaneous emission (ASE) noise. Fig. 7(a) shows the packet payload with remaining tags appearing at the unswitched port of the gate, whereas Fig. 7(b) shows the extracted tag #1 appearing switched at the gate output due to the interaction with the extracted packet clock. According to the principle of operation of ARTEMIS forwarding functionality, each routing bit embedded within the tag is accessed through the routing bit extraction gates. Fig. 7(d) shows the output of the first optical gate that performs Boolean AND operation between the single pulse extracted at the synchronization stage and the first routing bit in each packet tag. Depending on the binary value of these routing bits, a CW control signal is generated, as shown in Fig. 7(c), with duration equal to the packet length. These generated CW signals are used to control the all-optical 1×2 optical elements of the switching matrix described in the next section.

D. All-Optical Switching Matrix

The fundamental building block of the node-switching matrix is a 1×2 optically addressable switch implemented using SOA-MZI optical gates. Fig. 8(a) and (b) shows how these elementary 1×2 switching elements can be interconnected so as to form 4×4 and 8×8 strictly nonblocking switching matrices. As shown, the number of control signals required for the routing of a packet is equal to the number of stages within an N $\times$ N switching fabric, which is in turn equal to $T = \log_2 N$. In order to provide an independent optical path to interconnect each one of the inputs to every possible output a passive coupling stage is employed at the output of the Nth stage, consisting of N $\times$ 1 fiber couplers. The specific approach was chosen so as to be compatible with both the physical-layer design and control-plane algorithm: The switching matrix architecture is strictly nonblocking, ensuring that no internal

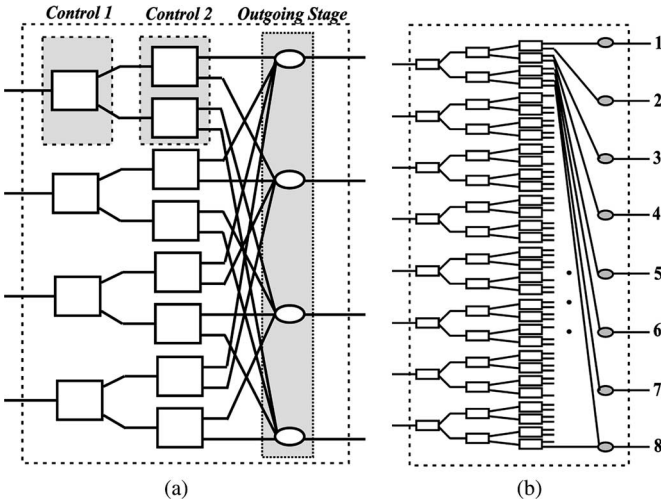

Fig. 8. ARTEMIS (a) 4 × 4 and (b) 8 × 8 switching matrices. In both cases, the elementary 1 × 2 switching elements are interconnected so as to form a strictly nonblocking switching fabric.

blocking occurs for input packets that arrive simultaneously at different input ports. On the other hand, the reservation signaling algorithm ensures that two incoming data packets do not request the same outgoing link, allowing for each output stage of the matrix to be coupled without causing contention.

Fig. 8 shows the 8 × 8 strictly nonblocking architecture designed for the self-routing node based on a tree approach. The propagation path of each incoming data packet within the array of interconnected optical gates depends on the CW control signals generated at the header-processing plane. At each stage, the presence of the CW control block changes the state of the 1 × 2 switch into cross state and the packet is switched accordingly towards the predetermined outgoing link. All eight incoming data packets are self-routed through the matrix in completely independent optical paths to avoid internal contention. At the output stage, the optical paths are coupled using 8 × 1 fiber couplers forming the outgoing links of the switching matrix.

The theoretical studies were focused on the noise performance of such a switching matrix due to cascade of SOA-MZI optical gates. In order to investigate the signal degradation of the optical packets, the simulation was used to model the propagation of the signal through the optically controlled 1 × 2 switches. Fig. 9(a) shows the incoming 40-Gb/s asynchronous data consisting of three asynchronous packets, each requesting a specific outgoing link. Fig. 9(b)–(d) shows pulse traces of the generated control signals for all packets at each stage in the switching matrix and Fig. 9(e)–(g) show the self-routed packets and corresponding eye diagrams. The eye diagrams of the routed optical packets at the ARTEMIS node outputs suffer primarily from amplitude noise, which is a direct consequence of the limited extinction ratio achievable from all-optical switching elements within the node. However, as shown in Fig. 9, the eye diagrams at the output of the switching matrix exhibit less timing jitter when compared to the eye diagrams of the incoming asynchronous packets. This effective retiming is achieved by the header/payload separation subsystem that exhibits regenerative properties, since the incoming packets are

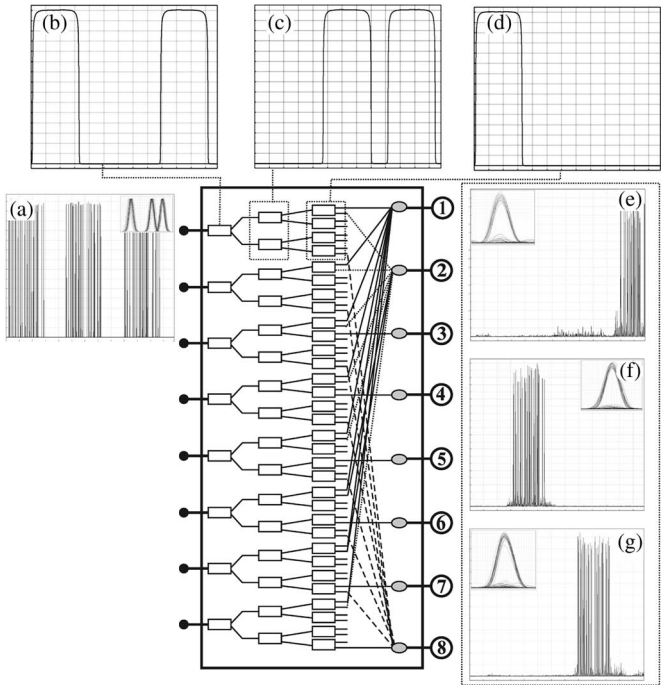

Fig. 9. Optical switching through the ARTEMIS 8 × 8 switching matrix. (a) Incoming 40-Gb/s asynchronous packets, (b), (c), (d) corresponding control signals generated, and (e), (f), (g) self-routed packets at the switch output.

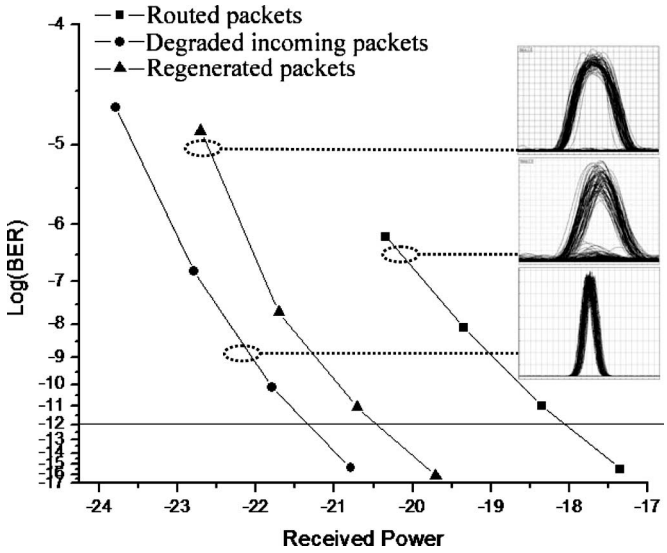

Fig. 10. BER measurements for degraded incoming packets, routed optical packets at the output of the 8 × 8 switch, and regenerated packets using two-stage 2R regenerator based on SOA-MZIs.

sampled with the retimed extracted clock packets [19]. Fig. 10 shows bit-error-rate (BER) measurements carried out in order to investigate the penalty induced due to signal propagation through cascaded optical switches, showing the BER of the incoming degraded data stream, the BER obtained at the output of the switching matrix for all packets, and finally, the BER after regeneration. The regenerator was modeled to be a two-stage 2R SOA-MZI and it effectively enhances the extinction ratio of the optical signal, as shown by the BER improvement in Fig. 10.

IV. ARTEMIS Control Plane

A. Contention Protection and Contention-Avoidance Mechanisms

Although self-routing is attractive due to the simplification of the routing control, the implementation of a bufferless, all-optical network requires a suitable control-plane design for the employment of contention control for traffic-engineering purposes. Data channel contention occurs when two or more packets/bursts are simultaneously destined to the same output port on the same wavelength. Standard methods to resolve this issue have been space deflection (deflection routing) [33]–[35], time deflection (buffering) [36], [37], and wavelength conversion [38].However, deflection routing affects the network load and cannot guarantee packet arrival in the correct order, time deflection is impractical due to the lack of scalable optical buffers while wavelength conversion raises the complexity of the node and thus the hardware cost. Moreover, none of the above policies are suitable for the all-optical self-router features of the ARTEMIS switching paradigm. On the other hand, optical protocols [39]–[42] have been proposed for connection establishment, which simultaneously provide contention protection by reserving resources during the connection establishment process. Within this context, source nodes are prevented from transmitting at overlapping periods or contending packets are being detected and discarded at intermediate nodes.

For the ARTEMIS concept, a signaling mechanism needs to be employed in order to resolve common output port contention of optical packets/bursts by communicating transmission periods, while the self-routing switching paradigm ensures correct intranode switching. The ability of the ARTEMIS switch for self-configuration makes the data plane architecture independent of the overlaying contention-protection signaling scheme and thus provides protocol transparency. Various reservation schemes have been proposed in the literature that can be categorized in two main classes, usually referred as one way (tell and go) [39], [40] and two way (tell and wait) reservation schemes [41], [42].

Within the context of ARTEMIS network, we are interested in one-way signaling schemes that employ timed/delayed reservations in order to maintain a low-delay overhead and efficiently utilize the available capacity. Since one wavelength is supported per link, specific channel scheduling algorithms [43], [52] are not required. However, in order to exploit the advantages of using timely network state information, a switching node must be capable of recording the periods when its outgoing links are reserved as a function of time, usually referred to as the "utilization profile" of the link [41]. In the proposed all-optical self-routing network, where no buffering and wavelength conversion is utilized, a burst requests the full bandwidth C of the single wavelength channels. Thus, we can represent the utilization profile of a link with a two-stated function of time with one state representing the reserved (OFF) and the other state the available periods of time (ON). Fig. 11 pictures the utilization profile of an ARTEMIS link, where the capacity is reserved on the link at time instances $t1$ and $t3$ for two data bursts/packets with durations equal to $|t2 - t1|$ and $|t4 - t3|$, respectively.

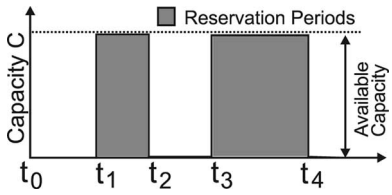

Fig. 11. Utilization profile of an ARTEMIS link.

In order to reduce network contention, we can proactively attempt to avoid network overloading through traffic management policies [44]–[48]. Contention-avoidance policies attempt to prevent a network from entering the congestion state in which packet/burst loss occurs. An ideal contention-avoidance policy must serve several concurrent objectives such as maximizing the throughput and minimizing the average end-to-end packet delay, while restraining the additional signaling requirements.

In general, contention-avoidance policies can be implemented in either nonfeedback-based or feedback-based algorithms. Nonfeedback algorithms employ traffic shaping in the IN [42]–[48] in order to reduce/normalize the incoming traffic burstiness. Since the IN has no knowledge of the network state, the main drawback of these algorithms is that they cannot respond to load and traffic changes of the network. On the other hand, a feedback-based network takes into account the global network load information and resource availability and contention avoidance is achieved by varying accordingly the data flows [44]–[46], [51]. Main issues in the feedback-based algorithms include defining the feedback mechanism and determining what type of information must be conveyed and to which source. It is worth noting that the main drawback of these algorithms is that when the round trip delay is large and the network operates at a very high speed, the edge nodes' responses to the network changes tend to be slow. Moreover, when alternative paths rerouting is employed there are cases that can lead to fluctuations and network instabilities.

In [45], the authors describe a feedback-based optical burst-switched (OBS) architecture in which core switch nodes send explicit messages to edge nodes requesting them to reduce their transmission rate on congested links and thus proactively attempts to prevent the network from entering the congestion state. The integration of contention resolution technique within the generalized multiprotocol label switching (GMPLS) framework is investigated in [44]. The proposed load-balancing technique is divided in two parts: 1) global network operation (using traffic engineering to reduce contention probability) and 2) local node layer operation (wavelength conversion and limited FDLs). In [46], a dynamic route selection technique using fixed alternate shortest paths and a least-congested dynamic route calculation technique are proposed to avoid congestions. In [51], the authors introduce a dynamic wavelength-routed OBS network architecture where centralized control is employed to ensure resource reservation efficiency while guaranteeing low delay and provide quality of service (QoS) differentiation.

For the ARTEMIS network, we are proposing a simple feedback-based contention-avoidance algorithm in which each

core node (CN) explicitly informs an IN for the acceptance and timing information (starting time and duration) of a burst only if this is useful by that specific IN. More specifically, each CN maintains a utilization profile of its outgoing links and informs IN ($T_{\text{CN-IN}}$ shortest path delay) for the acceptance of a burst with duration D after time ST only if $2 \cdot T_{\text{CN-IN}} <$ ST $+ D$. Additionally, for a network with N nodes, each IN needs to maintain a routing table with $N-1$ entries. Each entry contains the shortest path and a utilization profile that stores the timed/delayed reservations of that path links (addition by taking into account the propagation delays of the utilization profiles of the links that comprise the path). When an IN receives a state information message for a link, it updates all the utilization profiles of the paths that cross that link, taking into account the corresponding propagation delays in order to shift the reported temporal information. In the proposed feedback-based algorithm, an IN is informed only for the network state information that affects its operation and thus the required additional feedback signaling is constrained. Upon reception of a transmission request the IN searches the utilization profile for the specified destination in order to identify an adequate time offset for transmitting the packet/burst. It is worth noting that contentions can still occur when a burst is released on a path whose state has changed while this information did not manage to reach the IN on time. The proposed feedback-based contention-avoidance algorithm enables an ARTEMIS node to schedule the incoming requests in the time domain (perform void filling or future reservations) to avoid/prevent common output port contentions and increase the utilization of the available links. It is worth noting that in the case of the ARTEMIS network void filling is very efficient due to the minimal guardbands imposed by the physical layer.

Finally, based on the dynamic routing technique presented in previous section, we can implement a protection and fault tolerance mechanism [47]. When a link fails both end nodes of the failed link broadcast a failure-detection message throughout the network. Each IN will recompute a path for every path entry that crosses the failed link (and, respectively, initialize a new utilization profile for that new path).

B. Signaling and Load-Balancing Performance Evaluation

In this section, we show that a "tell and go" type of control protocols employing timed/delayed reservation of resources (only the latter feature is required) can be combined with the proposed feedback-based load-balancing algorithm to meet the objectives of the ARTEMIS network concept. We have extending the ns-2 platform [49] in order to simulate the basic features of the ARTEMIS switch and implement the proposed feedback-based load-balancing algorithm. Moreover, we have used the just-enough-time (JET) resource reservation protocol as provided by [50].

The simulations were conducted assuming two mesh topologies (3×3 and 6×6). In the mesh topologies, the nodes were arranged along a two-dimensional grid topology, with neighboring nodes placed at a distance of 200 km from each other. All links were assumed to be bidirectional, propagation delays were proportional to fiber lengths, header packet processing delay was set to 0.02 ms, and core bandwidth (C) was equal to 40 Gb/s. At each edge node, bursts transmission requests arrive following a Poisson process with rate λ requests per second and burst destinations were uniformly distributed over all nodes. Burst sizes (BSs) were assumed to follow an exponential distribution with mean value BS that corresponds to mean burst duration equal to: $\overline{T_{\text{data}}} = \text{BS}/C$. Typical mean burst transmission durations were considered (0.1–3 ms) that are equal or one order of magnitude less than the mean propagation delay of the networks ($\sim$ 2 ms for the 3×3 and $\sim$ 4 ms for the 6×6). Each edge router was modeled to employ a separate first in, first out (FIFO) queue per burst destination (virtual output queuing), with a total size of 256 MB.

We have simulated the JET reservation protocol with the Dijkstra shortest path selection algorithm and compare it with the proposed feedback-based contention-avoidance algorithm, as presented in the previous section. In order to evaluate the performance of the proposed all-optical self-router architecture in a network environment and compare the two aforementioned algorithms, we have considered the burst-loss ratio and average end-to-end delay as the main metrics for our simulation. Fig. 12(a)–(c) shows the corresponding results for the 3×3 mesh network while Fig. 12(b) and (d) presents the results obtained for the 6×6 mesh. In particular, Fig. 12(a) shows the burst-loss ratio and the corresponding average end-to-end delay of both algorithms as a function of the Poisson arrival rate (λ) for two average BSs (BS $= 1$ MB and BS $= 10$ MB), while Fig. 12(c) presents the same metrics as a function of BS, for two arrival rates ($\lambda = 40$ and $\lambda = 100$ requests per second). Fig. 12(b) and (d) presents the same simulation experiments for the 6×6 mesh network topology. As expected the blocking performance of both algorithms deteriorates as the offered load increases [increase of λ or BS—Fig. 12(a), (c) and (b), (d), respectively]. However, from these graphs it can be seen that in all cases the feedback-based contention-avoidance algorithm ensures a low burst-loss ratio with a small penalty in the end-to-end delay, a penalty that rises as the network load increases. By comparing the results obtained for the two different topologies, we can notice that the ARTEMIS concept combined with the proposed control plane under study is almost unaffected by the network size and thus we can deduce that the proposed architecture is scalable. The results obtained for the JET reservation scheme with the proposed feedback-based contention-avoidance algorithm show that it is feasible to accommodate the self-routing switching concept of the ARTEMIS network by successfully preventing contentions. The acceptable performance in terms of dropping probability and end-to-end delay validates the "protocol transparency" and provide a base case for defining how end-user service requirements can be supported. It is worth noting that the study presented in this section should be considered as a proof of the operation of the ARTEMIS concept on the network level. Further studies of the resource reservation/contention prevention schemes and contention-avoidance algorithms are required in order to optimize the ARTEMIS network performance and propose suitable QoS differentiation mechanisms.

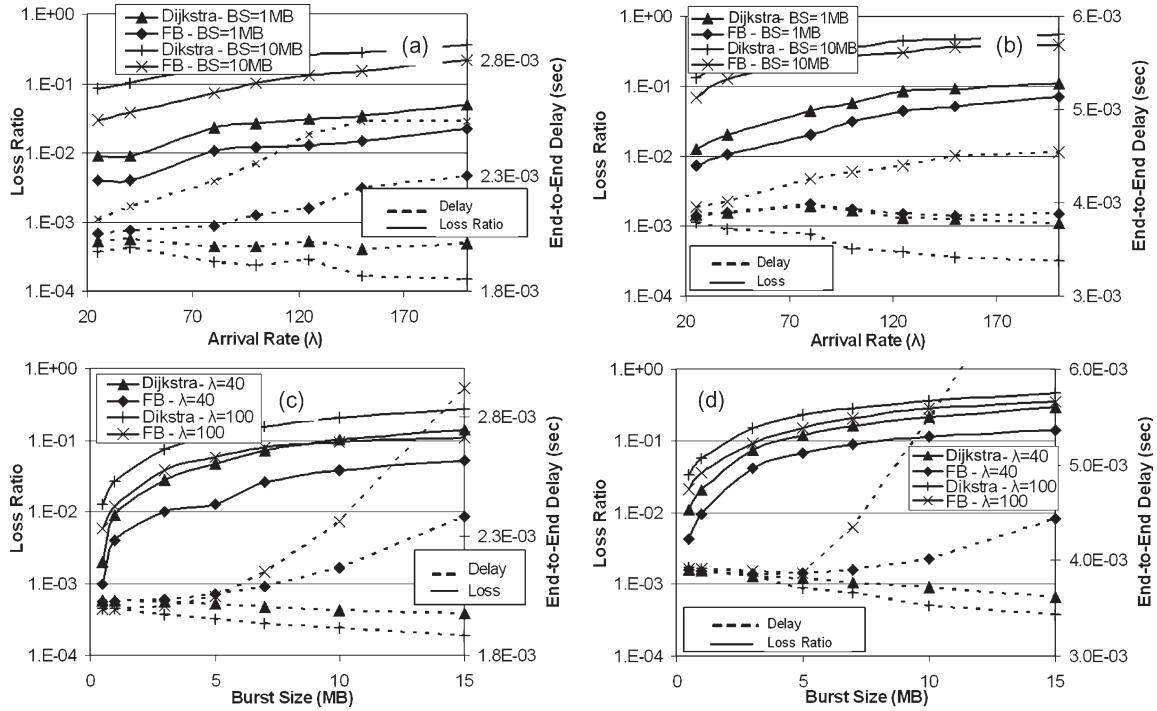

Fig. 12. (a) Loss ratio and average end-to-end delay as function of Poisson arrival rate (λ), for two average BS values, and (c) loss ratio and average end-to-end delay as function of average BS for two different λ values for the 3×3 mesh network. (b) and (d) same graphs for the 6×6 network. Dijkstra stands for the JET reservation scheme with the Dijkstra simple shortest path selection algorithm, while FB stands for the feedback-based contention-avoidance algorithm proposed for the ARTEMIS concept.

V. Conclusion

We have demonstrated for the first time a complete 40-Gb/s asynchronous self-routing-network architecture and validated the proposed concept through network studies and node physical-layer simulations. The ARTEMIS concept relies on all-optical self-routing of optical packets on a hop-by-hop basis by using stacked optical tags, each representing a specific optical node. According to the proposed concept, transmission, regeneration, and routing of data are performed solely in the optical layer, whereas the electrical control plane is only responsible for resources reservation and connection establishment.

In the physical layer, each ARTEMIS node subsystem responsible for synchronization, header processing and switching was individually modeled using a commercial simulation tool. The proposed proof of principle was validated for a complete 8×8 all-optical self-router, focusing on signal quality and BER. The number of hops possible using 2R regenerator is limited, primarily due to pulse broadening induced by the SOA recovery time in the 2R-regenerator stage. However, the number of hops can be significantly increased by employing reshaping, reamplification, and retiming (3R) regeneration, using the all-optical clock recovery proposed in ARTEMIS for retiming and reshaping the data traffic [53]. The ARTEMIS network concept was also investigated by simulating the control plane of such a network, showing acceptable performance when both two-way and one-way timed reservation of resources is applied.

ARTEMIS nodes can achieve high bit-rate operation though on-the-fly all-optical signal processing techniques, without employing any dynamic buffering. Hop-by-hop routing is performed solely in the optical layer through address information embedded in the packet header at the IN, avoiding O/E/O conversions, lookup tables, and high-speed electronic processing. In addition, the ARTEMIS network can provide high throughput and low blocking ratio when combined with appropriate resource reservation sign4ling scheme and load-balancing contention-avoidance mechanisms. The optical layer, on the other hand, provides a high transmission efficiency for packets as short as a few nanoseconds, verifying the node compatibility to true all-optical packet switching. Considering future data-centric photonic networks, where even control-plane functionalities are performed in the optical layer, ARTEMIS can provide very fine granularity and operate transparently to network traffic and packet format [30].

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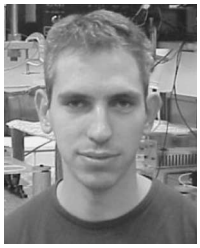

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